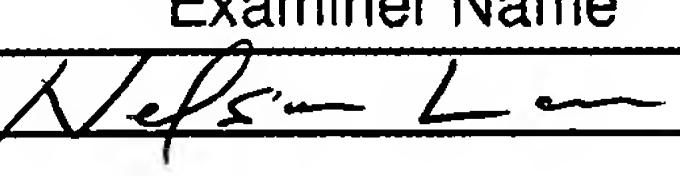
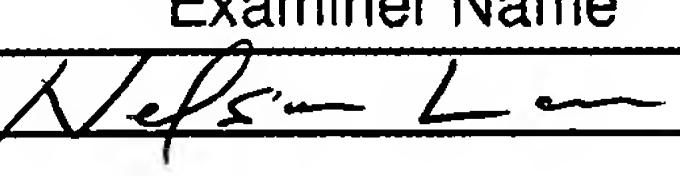
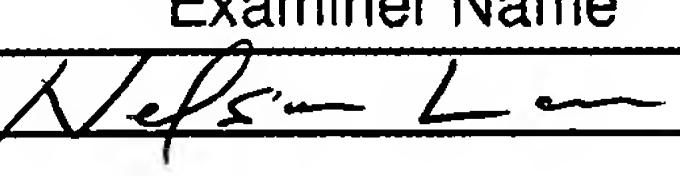


INFORMATION DISCLOSURE CITATION <i>(Use several sheets if necessary)</i>		Docket Number (Optional) BUR920030135US1	Application Number 10/709292 Not Yet Assigned
		Applicant(s) Allen et al.	
		Filing Date 04/27/04 Concurrently Herewith	Group Art Unit Unknown
*EXAMINER INITIAL	OTHER DOCUMENTS <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>		
 NL	Papadopoulou, E. and Lee, D.T., "Critical area computation via Voronoi diagrams," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, Vol. 18, No. 4, pp .463-474, April 1999.		
	Papadopoulou, E., "Critical area computation for missing material defects in VLSI circuits," Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, Vol. 20, No. 5, pp 583-597, May 2001.		
NL	Fook-Luen Heng and Zhan Chen. "VLSI Yield Enhancement Techniques Through Layout Modification." IBM T. J. Watson Research Center, pp. 1-15, July 17, 2000.		
NL	A. Venkataraman and I. Koren. "Trade-offs between Yield and Reliability Enhancement." Proc. of the 1996 IEEE National Symposium on Defect and Fault Tolerance in VLSI Systems, pp. 67-75, November 1996.		
EXAMINER	DATE CONSIDERED		
<i>Nels L</i>	<i>8/29/06</i>		
*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.			

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Title of Invention	INTEGRATED CIRCUIT YIELD ENHANCEMENT USING VORONOI DIAGRAMS																																						
<p>Application Number : Confirmation Number: First Named Applicant: Robert Allen Attorney Docket Number: BUR920030135US1 Art Unit: Examiner: Search string: (6178539 or 6247853 or 6317859).pn</p>																																							
<h3>US Patent Documents</h3> <p>Note: Applicant is not required to submit a paper copy of cited US Patent Documents</p> <table border="1"><thead><tr><th>init</th><th>Cite.No.</th><th>Patent No.</th><th>Date</th><th>Patentee</th><th>Kind</th><th>Class</th><th>Subclass</th></tr></thead><tbody><tr><td>NL</td><td>1</td><td>6178539</td><td>2001-01-23</td><td>Papadopoulou et al.</td><td></td><td></td><td></td></tr><tr><td>NL</td><td>2</td><td>6247853</td><td>2001-06-19</td><td>Papadopoulou et al.</td><td></td><td></td><td></td></tr><tr><td>NL</td><td>3</td><td>6317859</td><td>2001-11-13</td><td>Papadopoulou et al.</td><td></td><td></td><td></td></tr></tbody></table>								init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass	NL	1	6178539	2001-01-23	Papadopoulou et al.				NL	2	6247853	2001-06-19	Papadopoulou et al.				NL	3	6317859	2001-11-13	Papadopoulou et al.			
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<p>Signature</p> <table border="1"><tr><td>Examiner Name</td><td>Date</td></tr><tr><td></td><td>8/29/06</td></tr></table>								Examiner Name	Date		8/29/06																												
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